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EXAMINER	
ROSENDALE, MATTHEW L	
ART UNIT	**PAPER NUMBER**
2612	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/393,311	FOX, ERIC	
	Examiner	Art Unit	
	Matthew L Rosendale	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,16-22 and 38* is/are allowed.

6)☒ Claim(s) *2-5,9-15 and 23-37* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

In response to the applicants arguments as to the rejection of claims under 35 U.S.C. 112, first paragraph, the examiner agrees with the applicant that only one embodiment needs to have support in the specification and therefore the rejection will be withdrawn.

Applicant's arguments regarding claims 24 – 37, filed 1/20/04 have been fully considered but they are not persuasive. Referring to claims 24 and 34, the applicant argues that Audier et al fails to teach or suggest all claimed features, specifically, incrementing the first switch control circuit and a third switch control circuit to output an accumulated value from the column of accumulators.

The examiner reminds the applicant that claims 24 and 34 have two distinct interpretations and that there is no specific sequence claimed in the method claim of 24 or the sensor means for claim of 34. Therefore in the rejection of claims 24 and 34, the limitations were interpreted in the following. First the column of accumulators from a column of pixels is updated by repeatedly incrementing first and second switch control circuits. Then a third switch control circuit is incremented to output an accumulated value from the column of accumulators. Then the first switch control circuit is once again incremented to start the process over (Col. 2, Line 39 – Col. 3, Line 57).

It is also pointed out by the examiner that as currently claimed, the limitation of incrementing the first switch control circuit and a third switch control circuit to output an

accumulated value from the column of accumulators has two interpretations. The first interpretation is argued by the application where outputting an accumulated value from the column of accumulators involves incrementing BOTH the first switch control circuit and a third switch control circuit.

However, in the rejection of claims 24 and 34 the examiner relied on the second interpretation where incrementing the first switch control circuit and incrementing a third switch control circuit are two distinct, separate, and non sequential steps where only the third switch control circuit is incremented to output an accumulated value from the column of accumulators. Therefore the rejection of claims 24 and 34 will be maintained as being anticipated by Audier et al.

In response to the applicants' traversal of the Official Notice taken in the rejection of claim 23, a reference will be provided as requested by the applicant. However, providing a reference in response to a traversal of Official Notice does not merit a second non-final rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 24 – 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Audier et al.

Referring to claim 24, Audier discloses a method of scanning an image comprising steps of:

updating a column of accumulators from a column of pixels by repeatedly incrementing first and second switch control circuits; and

incrementing the first switch control circuit and a third switch control circuit to output an accumulated value from the column of accumulators.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp.

After the nth cycle of incrementing the first and second switch sets to output a plurality of signals from each pixel in the column to their corresponding accumulator Cp updating the signal stored therein, the contents of each accumulator are extracted to the output bus by incrementing the third switches Slec(p) coupling the output of each accumulator Cp to the output bus (Col. 2, Line 39 – Col. 3, Line 57).

2. Referring to claim 25, Audier discloses the method of claim 24, wherein the step of updating a column of accumulators includes steps of:

transferring a pixel signal from a pixel selected from the column of pixels based on the first switch control circuit into an accumulator selected from the column of accumulators based on the second switch control circuit; and

updating the selected accumulator.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

3. Referring to claim 26, Audier discloses the method of claim 25, wherein the step of updating a column of accumulators further includes:

a step of causing the step of transferring a pixel signal from a pixel to successively repeat; and

a step of causing the step of updating the selected accumulator to successively repeat to update each accumulator in the column of accumulators.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij

to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles of incrementing the first and second switches so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

4. Referring to claim 27, Audier discloses the method of claim 25, wherein the step of transferring a pixel signal includes:

addressing the selected pixel based on the first switch control circuit to transfer a selected pixel signal from the selected pixel onto a column bus; and

addressing the selected accumulator based on the second switch control circuit to transfer the selected pixel signal from .the column bus into the selected accumulator.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the

sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

5. Referring to claim 28, Audier discloses the method of claim 27, wherein the step of updating the selected accumulator includes updating an accumulator signal value stored in the selected accumulator based on the selected pixel signal.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp.

6. Referring to claim 29, Audier discloses the method of claim 24, further comprising a step of causing the steps of updating a column of accumulators and incrementing the first switch control circuit and a third switch control circuit to output an accumulated value to successively repeat.

After the nth cycle of incrementing the first and second switch sets to output a plurality of signals from each pixel in the column to their corresponding accumulator Cp updating the signal stored therein, the contents of each accumulator are extracted to the output bus by incrementing

the third switches Slec(p) coupling the output of each accumulator Cp to the output bus (Col. 2, Line 39 – Col. 3, Line 57).

7. Referring to claim 30, Audier discloses the method of claim 24, wherein the step of incrementing the first switch control circuit and a third switch control circuit to output an accumulated value includes transferring the accumulated value from an accumulator selected from the column of accumulators based on the third switch control circuit onto an output bus.

After the nth cycle of incrementing the first and second switch sets to output a plurality of signals from each pixel in the column to their corresponding accumulator Cp updating the signal stored therein, the contents of each accumulator are extracted to the output bus by incrementing the third switches Slec(p) coupling the output of each accumulator Cp to the output bus (Col. 2, Line 39 – Col. 3, Line 57).

8. Referring to claim 31, Audier discloses a sensor comprising:

means for updating a column of accumulators from a column of pixels by repeatedly incrementing first and second switch control circuits; and

means for incrementing the first switch control circuit and a third switch control circuit to output an accumulated value from the column of accumulators.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp.

After the Nth cycle of incrementing the first and second switch sets to output a plurality of signals from each pixel in the column to their corresponding accumulator Cp updating the signal stored therein, the contents of each accumulator are extracted to the output bus by incrementing the third switches Slec(p) coupling the output of each accumulator Cp to the output bus (Col. 2, Line 39 – Col. 3, Line 57).

9. Referring to claim 32, Audier discloses the sensor of claim 31, wherein the means for updating a column of accumulators includes:

means for transferring a pixel signal from a pixel selected from the column of pixels based on the first switch control circuit into an accumulator selected from the column of accumulators based on the second switch control circuit; and

means for updating the selected accumulator.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the

sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

10. Referring to claim 33, Audier discloses the sensor of claim 32, wherein the means for updating a column of accumulators further includes:

means for causing the means for transferring a pixel signal from a pixel to successively repeat; and

means for causing the means for updating the selected accumulator to successively repeat to update each accumulator in the column of accumulators.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

11. Referring to claim 34, Audier discloses the sensor of claim 32, wherein the means for transferring a pixel signal includes:

means for addressing the selected pixel based on the first switch control circuit to transfer a selected pixel signal from the selected pixel onto a column bus; and

means for addressing the selected accumulator based on the second switch control circuit to transfer the selected pixel signal from the column bus into the selected accumulator.

As disclosed, the sequencer logic of Audier addresses a selected pixel by closing a first switch Iij coupling the selected pixel to the column bus shown in figure 1. The accumulator Cp in figure 2 is addressed by closing a second switch Ssom(p) coupling the accumulator Cp to the column bus to receive the pixel signal output from the corresponding pixel in the column (Col. 2, Line 39 – Col. 3, Line 57).

12. Referring to claim 35, Audier discloses the sensor of claim 34, wherein the means for updating the selected accumulator includes means for updating an accumulator signal value stored in the selected accumulator based on the selected pixel signal.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

13. Referring to claim 36, Audier discloses the sensor of claim 31, further comprising means for causing the steps of updating a column of accumulators and incrementing the first switch control circuit and a third switch control circuit to output an accumulated value to successively repeat.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp.

After the nth cycle of incrementing the first and second switch sets to output a plurality of signals from each pixel in the column to their corresponding accumulator Cp updating the signal stored therein, the contents of each accumulator are extracted to the output bus by incrementing the third switches Slec(p) coupling the output of each accumulator Cp to the output bus (Col. 2, Line 39 – Col. 3, Line 57).

14. Referring to claim 37, Audier discloses the sensor of claim 31, wherein the means for incrementing the first switch control circuit and a third switch control circuit to output an accumulated value includes means for transferring the accumulated value from an accumulator selected from the column of accumulators based on the third switch control circuit onto an output bus.

After the nth cycle of incrementing the first and second switch sets to output a plurality of signals from each pixel in the column to their corresponding accumulator Cp updating the signal stored therein, the contents of each accumulator are extracted to the output bus by incrementing

the third switches Slec(p) coupling the output of each accumulator Cp to the output bus (Col. 2, Line 39 – Col. 3, Line 57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2 – 5, 9 – 13, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Audier et al in view of Malhi.

Referring to claim 23, Audier discloses an image sensor in figure 1 comprising:

a column bus;

a column of pixels Cij;

a first plurality of switches Iij, each switch being coupled between the column bus and a corresponding pixel of the column of pixels Cij;

a column of accumulators C1 - CM in figure 2;

a second plurality of switches Ssom(p) in figure 2, each switch being coupled between the column bus and a corresponding accumulator Cp of the column of accumulators;

a main control circuit to control the first Iij and second Ssom(p) plurality of switches to couple a signal from a pixel of the column of pixels Cij to an accumulator Cp of the column of accumulators C1 – CM while updating the accumulator Cp (Col. 2, Lines 39 – 61 and Col. 3, Lines 38 – 57).

Audier does not disclose that the column bus, all pixels in the column of pixels, a switches of the first and second plurality of switches, all accumulators in the column of accumulators, and the main control circuit include poly-crystalline silicon conductors, all poly-crystalline silicon conductors being formed from only a single layer of a patterned poly-crystalline silicon film.

However, Malhi discloses that it is well known in the art of CMOS fabrication to use a poly-crystalline silicon conductors formed of a signal layer of silicon film. Figures 1a – 1c of Malhi illustrate a CMOS fabrication process where a single layer of poly-crystalline silicon 11 is formed on a substrate and N+ doped poly-crystalline silicon conductors are etched from the signal layer to form the CMOS device.

Therefore it would have been obvious to use poly-crystalline silicon conductors formed on a signal layer of silicon film as a means of fabricating the image sensor of Audier with high component density.

16. Referring to claim 2, Audier discloses the sensor of claim 1, wherein the main control circuit includes:

a first switch control circuit to control a switch of the first plurality of switches to connect the signal from the pixel of the column of pixels to the column bus while controlling all remaining switches of the first plurality of switches to isolate the column bus from all remaining pixels of the column of pixels; and

a second switch control circuit to control a switch of the second plurality of switches to connect the signal on the column bus to the accumulator of the column of

accumulators while controlling all remaining switches of the second plurality of switches to isolate the column bus from all remaining accumulators of the column of accumulators (Col. 3, Lines 38 – 57).

As disclosed the sequencer logic of Audier controls a multiplexer to sequentially transfer Nd current pulse from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

17. Referring to claim 3, Audier discloses the sensor of claim 2, wherein the main control circuit further includes:

a first increment control circuit to increment the first switch control circuit to control a next in succession switch of the first plurality of switches to connect a signal from a next in succession pixel of the column of pixels to the column bus while controlling all remaining switches of the first plurality of switches, to isolate the column bus from all remaining pixels of the column of pixels; and

a second increment control circuit to increment the second switch control circuit to control a next in succession switch of the second plurality of switches to connect the signal on the column bus to a next in succession accumulator of the column of accumulators while controlling all remaining switches of the second plurality of switches to isolate the column bus from all remaining accumulators of the column of accumulators (Col. 3, Lines 38 – 57).

As disclosed the sequencer logic of Audier controls a multiplexer to sequentially transfer Nd current pulse from the pixel sensors in the column of pixel sensors Cij to their corresponding

accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp.

18. Referring to claim 4, Audier discloses the sensor of claim 3, wherein the main control circuit further includes a first repeat control circuit to repetitively operate the first increment control circuit, the first switch control circuit, the second increment control circuit, and the second switch control circuit;

each repetitive operation of the first switch control circuit couples a signal from a successive pixel of the column of pixels onto the column bus; and

each repetitive operation of the second switch control circuit couples the signal that was coupled onto the column bus from a pixel to a corresponding accumulator of the column of accumulators.

As disclosed the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulse from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp. Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

19. Referring to claim 5, Audier discloses the sensor of claim 4, wherein each time the first repeat control circuit is operated, the first repeat control circuit:

repetitively operating the first increment control circuit and the first switch control circuit until all pixels of the column of pixels have been successively coupled onto the column bus; and

repetitively operates the second increment control circuit and the second switch control circuit until the signal on the column bus has been successfully coupled into all accumulators of the column of accumulators.

As disclosed the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulse from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp. Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

20. Referring to claim 9, Audier discloses the sensor of claim 1 further comprising: an output bus shown in figure 2;

a third plurality of switches Slec(p), each switch being coupled between the output bus and a corresponding accumulator of the column of accumulators C1 - CM, wherein the main control circuit controls the third plurality of switches to couple an accumulated signal from an

accumulator CP of the column of accumulators C1 – CM to the output bus (Col. 3, Lines 38 – 63).

21. Referring to claim 10, Audier discloses the sensor of claim 9, wherein the main control circuit includes a switch control circuit to control a switch of the third plurality of switches Slec(p) in figure 2, to connect the accumulated signal from the accumulator CP of the column of accumulators C1 – CM to the output bus while controlling all remaining switches of the third plurality of switches Slec(p) to isolate the output bus from all remaining accumulators of the column of accumulators C1 – CM (Col. 3, Lines 38 – 63).

As discloses by Audier, the sequencer circuit extracts the contents of each accumulator by closing the third switch Slec(p) coupling the selected accumulator to the output bus.

22. Referring to claim 11, Audier discloses the sensor of claim 10, wherein the main control circuit further includes an increment control circuit to increment the switch control circuit to control a next in succession switch of the third plurality of switches Slec(p) to connect the accumulated signal at a next in succession accumulator of the column of accumulators C1 – CM to the output bus to while controlling all remaining switches of the third plurality of switches Slec(p) to isolate the output bus from all remaining accumulators of the column of accumulators C1 – CM (Col. 3, Liens 38 – 63).

As discloses by Audier, the sequencer circuit extracts the contents of each accumulator by closing the third switch Slec(p) coupling the selected accumulator to the output bus.

23. Referring to claim 12, Audier discloses the sensor of claim 11, wherein the main control circuit further includes a repeat control circuit to repetitively operate the increment control circuit and the switch control circuit; and each repetitive operation of the switch control circuit couples a signal from a successive accumulator of the column of accumulators.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp. Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

24. Referring to claim 13, Audier discloses the sensor of claim 12, wherein each time the repeat control circuit is operated, the repeat control circuit repetitively operates the increment control circuit and the switch control circuit until all accumulators CP of the column of accumulators C1 – Cm in figure 2 have been successively coupled onto the output bus.

As disclosed, the sequencer logic of Audier controls a multiplexer to sequentially and repetitively transfer Nd current pulses from the pixel sensors in the column of pixel sensors Cij to their corresponding accumulator Cp by sequencing the first Iij and second Ssom(p) switches coupling a pixel sensor to the column bus and the column bus to the accumulator Cp. Audier discloses that the sequence for transferring pixel signals to the accumulators is repeated for N

cycles so that the charge stored in each accumulator C1 – CM corresponds to the sum of the current samples Id(k) output on the column bus from each pixel sensor to their corresponding accumulator Cp (Col. 2, Line 39 – Col. 3, Line 57).

25. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Audier in view Malhi in further view of Hunt et al.

Referring to claim 14, Audier discloses a TDI (time delay integration) CMOS sensor. Audier does not disclose that the main control circuit operates the repeat control circuit each time a point in a moving image projected on the column of pixels transverses a pixel boundary. However, Hunt discloses that it is well known to use TDI type image sensors for imaging objects on a conveyer belt having a fixed time interval (Col. 3, Lines 6 – 49).

Therefore it would have been obvious to one of ordinary skill in the art to read each line of the sensor as the object being imaged passes each pixel row so as to record as much object data as possible with each passing row of the TDI image sensor.

26. Referring to claim 15, Audier discloses a TDI (time delay integration) CMOS sensor. Audier does not disclose that the main control circuit repetitively operates the repeat control circuit until the point in the moving image traverses the column of pixels. However, Hunt discloses that it is well known to use TDI type image sensors for imaging objects on a conveyer belt having a fixed time interval (Col. 3, Lines 6 – 49).

Therefore it would have been obvious to one of ordinary skill in the art to set the operating cycle of the image sensor to the interval of the object being imaged thereby allowing

the image sensor to capture image data of the object passing through the column of sensors then resetting the image sensor in the time between imaging the current object and the next object.

Allowable Subject Matter

Claims 7, 8, 16 – 22, and 38 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Referring to claim 38, the prior art fails to teach or suggest a second repeat control circuit to operate the first increment control circuit and then operate the first repeat control circuit each time the second repeat control circuit is operated.

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 6, the prior art fails to teach or suggest a second repeat control circuit to operate the first increment control circuit and then operate the first repeat control circuit each time the second repeat control circuit is operated.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew L Rosendale whose telephone number is (703) 305-4909. The examiner can normally be reached on Monday - Friday 8: 00am-4: 00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MLR

NGOC-YEN VU
PRIMARY EXAMINER